ABSTRACT OF THE DISCLOSURE

One or more methods and systems of resynchronizing or dynamically re-tuning a clock signal over a high speed clocked data interface are presented. In one embodiment, the system and method utilizes first and second delay lines, a first pair of digital logic devices to generate a first data sequence, a second pair of digital logic devices to generate a second data sequence, a memory, a set of software instructions resident in the memory, a processor, and a user interface. The first and second data sequences are input into a digital logic circuit that compares the two sequences and generates an output. The output is clocked into a digital logic device to generate an indicator signal that is used to resynchronize or dynamically re-tune the clock signal.